

Appl. No. 09/809,181  
Amendment dated December 19, 2003  
Reply to Office Action of June 19, 2003

### **REMARKS**

Claims 1-10 and 28-36 are pending in this application. No claim has been amended herein.

Claims 1 and 5 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the Examiner asserts that claims 1 and 7 recite a means plus function limitation, which is **not** clear and, as a result, will be interpreted as merely any step that result in a diced semiconductor structure having a stress cushioning layer, a lead wire portion, a conductive protective layer, and external electrodes. However, the Examiner's assertion is factually incorrect. Base claims 1 and 7 each defines,

**"wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."**

There is nothing unclear regarding the above limitation. Means-plus-function limitation is permitted under 35 U.S.C. §112, 6<sup>th</sup> paragraph, to capture all means and its equivalent to perform two recited functions: (1) forming each end face on an end surface of said semiconductor elements inside said cutting scribe line; and (2) exposing a range of said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line. More importantly, these recited functions are performed in such a way that "said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."

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As can be seen from Applicants' base claims 1 and 5, these recited functions are clear and definite to one skilled in the art and, certainly, in compliance with 35 U.S.C. §112, 2<sup>nd</sup> paragraph. Therefore, the Examiner's interpretation of the means-plus-function clause is incorrect and should be reassessed.

Separately, the Examiner also asserts that,

the term "end face" is indefinite since no structure relationship can be determined between the stress-cushioning layer, lead wire, conductive protective layer, semiconductor elements, semiconductor element protective layer, cutting scribe line and external electrodes. It is not clear whether the term "end face" is used to indicate a top or bottom surface of each layer, e.g., the stress-cushioning layer, lead wire, conductive protective layer, semiconductor elements, semiconductor element protective layer, cutting scribe line and external electrodes."

Again, the assertion is simply baseless. There is nothing value or indefinite regarding the term "end face" in a context of "an end surface of said semiconductor elements." The word "end" is defined in the Webster's New World Dictionary as "the part at, toward, or near either of the extremities of anything; tip" or "boundary". The word "face" is defined in the Webster's New World Dictionary as "a surface of a thing." When read in the context of "an end surface of said semiconductor elements," such the "end face" is nothing more than the end face of the end surface of the semiconductor elements and, contrary to the Examiner's misleading reading, does not mean nor is used to indicate a top or bottom surface of each layer.

Accordingly, in view of the foregoing explanations and inherent meaning of the terms as expressly defined in Applicants' base claims 1 and 5, Applicants respectfully request that the rejection of Applicants' base claims 1 and 5 under 35 U.S.C. §112, second paragraph, be withdrawn.

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Lastly, claims 1-10 and claims 28-36 have been rejected under 35 U.S.C. §102(b) as being anticipated by Yamamoto Tetsuhiro, JP 10-0928654 for reasons stated on pages 3-5. However, the Examiner's assertion is factually incorrect and legally improper. Applicants submit that key features of Applicants' claims 1-10 and 28-36 have been conveniently ignored by the Examiner and, more importantly, are not disclosed anywhere in Yamamoto '865. As a result, Applicants respectfully request the Examiner to reconsider and withdraw these rejections for the following reasons.

First of all, in rejecting Applicants' claims 1-10 and 28-36 under any statutory authority, the Examiner bears the initial burden of establishing a *prima facie* case of anticipation. Only if this burden is met does the burden of coming forward with rebuttal argument or evidence shift to the Applicants. In Ex parte Levy, 17 USPQ2d 1461, 1462 (1990), the Court expressly states that:

"it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

In addition, 37 CFR §1.106(b) requires the Examiner, when rejecting claims for want of novelty, must cite the best references at his command. When a reference is complex or shows or describes inventions other than that claimed by the Applicants, the particular part relied upon must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

More importantly, the rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be

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disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

The burden of establishing a basis for denying patentability of a claimed invention rests upon the Examiner. The limitations required by the claims cannot be ignored. See In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). All claim limitations, including those which are functional, must be considered. See In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981). Hence, all words in a claim must be considered in deciding the patentability of that claim against the prior art. Each word in a claim must be given its proper meaning, as construed by a person skilled in the art. Where required to determine the scope of a recited term, the disclosure may be used. See In re Barr, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

In the present situation, not only the Examiner has completely ignored key limitations of Applicants' claims 1-10 and 28-36, but has also failed to show how each and every element of Applicants' claims 1-10 and 28-36 is disclosed in Yamamoto '865. Furthermore, not Yamamoto '865 fails to disclose all features of

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Applicants' claims 1-10 and 28-36 but only serves as background art of Applicants' disclosed invention. Specifically, on page 5, lines 5-12 of Applicants' original disclosure, Applicants cite Yamamoto '865 for disclosing:

"a semiconductor device of a type in which a resin layer for cushioning stress is installed between external electrodes and semiconductor elements. Individual semiconductor devices are manufactured by processing units of semiconductor wafer in a batch and finally cutting each semiconductor wafer into pieces."

The problem of this type of semiconductor device as described by Yamamoto '865 is that,

"a plurality of resin layers and external electrodes are formed in units of semiconductor wafers in a batch, and then each semiconductor wafer is cut (diced) into pieces, has a constitution such that the interfaces of a plurality of resin layers sequentially formed on each semiconductor wafer are exposed on the end face of each semiconductor package, so that when a large mechanical stress is applied to the interfaces of the plurality of resin layers at the time of dicing of the semiconductor wafer, or when a large thermal stress is applied to the interfaces of the plurality of resin layers due to sudden temperature changes at the time of mounting of the semiconductor package, the stress is centralized to the interfaces between the semiconductor element exposed on the end face of the semiconductor package and the plurality of resin layers, so that one or more of the plurality of resin layers are peeled off and the semiconductor package may be damaged.

As mentioned above, such a known semiconductor device cannot always exhibit high reliability, and it is difficult to obtain a high manufacturing yield rate." See pages 5-6 of Applicants' original disclosure.

Because of the problems associated with Yamamoto '865, Applicants propose a solution, a semiconductor device in which a semiconductor element has at least a stress cushioning layer and a semiconductor protective layer, and end faces of these layers are positioned inside the cutting scribe lines formed on a semiconductor wafer, and the range of the surface at the end of the semiconductor element from the



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end face to the inside of the scribe line is exposed, see page 1, lines 5-15 of

Applicants' original disclosure.

This arrangement is intended so as the semiconductor device within an individual dice to withstand the concentrated stress applied at the time of cutting a semiconductor wafer into a plurality of dices and at the time of mounting a semiconductor device in order to minimize damage due to the applied stress and thereby obtaining high reliability and manufacturing yield rate, see page 6, lines 16-25 of Applicants' original disclosure.

Specifically, independent claim 1 expressly defines a semiconductor device comprising:

"semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion, wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."

Likewise, independent claim 5 defines a semiconductor device comprising:

"semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line,  
a semiconductor element protective layer installed on said semiconductor elements,  
a stress cushioning layer installed on said semiconductor element protective layer,

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a first opening formed in said semiconductor element protective layer on said electrode pad,  
a second opening formed in said stress cushioning layer on said electrode pad,  
a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad,  
external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and  
a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,  
wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."

Likewise, independent claim 33 defines a semiconductor device comprising:

at least one semiconductor element including an electrode pad formed on one side along a cutting scribe line;  
a stress cushioning layer formed on said semiconductor element;  
a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad;  
external electrodes installed on said lead wire portion on top of said stress cushioning layer; and  
a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,  
wherein each end face of said stress cushioning layer, and said conductor protective layer is formed on an end surface of said semiconductor element so as to be positioned inside said cutting scribe line and to be exposed within a range from said end face on said end surface of said semiconductor element to an inside of said cutting scribe line.

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As expressly defined in each of Applicants' base claims 1, 5 and 33, each end face of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), is formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line.

This is necessary so that when a semiconductor wafer is to be cut along the cutting scribe line, the semiconductor wafer can be cut without any damage to semiconductor devices within the cutting scribe line due to application of mechanical stress and thermal stress in order to enhance reliability of the semiconductor devices and increase the production yield rate of the semiconductor devices. See pages 9-10 of Applicants' substitute specification.

In contrast to Applicants' independent claims 1, 5 and 33, Yamamoto '865 discloses none of these features, as expressly acknowledged in the background of Applicants' original disclosure.

Nevertheless, in support of the rejection of Applicants' claims 1, 5 and 33, the Examiner simply asserts that Yamamoto '865 teaches,

"a semiconductor device (see entire disclosure) comprising an electrode pad (13), a stress cushioning layer 917), a lead wire (14), external electrodes (11), and a conductor protective layer (10) (see Figs. 1-2)."

Notwithstanding the fact that the Examiner has ignored all the essential features of Applicants' independent claims 1, 5 and 33, Yamamoto '865, as discussed previously, addresses a different problem and the solution disclosed by



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Yamamoto '865 has problems which are the reasons for Applicants' disclosed invention.

Specifically, Yamamoto '865 proposes to prevent a semiconductor element with a small number of pins such as a memory, a general-purpose microcomputer, etc., from becoming expensive and the miniaturization rate of QFP from becoming small, even if it is made into CSP (chip size package). See Abstract.

For this purpose, the metallic wiring 14 drawn out of the element electrode 13 of a semiconductor element 12 is made on a first resin layer 15, as shown in FIG.2, and the element electrode 13 of the semiconductor element 12 and a package electrode 11 are electrically connected with each other through the metallic wiring 14. Then, the electric connection with outside is performed at the package electrode 11 positioned in the opening of a second resin layer 10. Moreover, the stress caused by the difference of thermal expansion between a mounting board and the silicon (Si) of the semiconductor element 12 when this semiconductor device and an outside mounting board are mounted is relieved by the polyimide resin layer 17, a first resin layer 15, and a second resin layer 10 made on a passivation film 16. Thus, the chip size package (CSP) can be manufactured at lowcost, because they are processed en block in wafer units without performing individual assembly.

While some elements of Yamamoto '865 may be considered as similar to some of Applicants' elements as defined in independent claims 1, 5 and 33, the configuration, arrangement and functions of Yamamoto '865 and Applicants' claimed invention are completely different.

For example, and for the Examiner's convenience, the element electrode 13, as shown in FIG. 2 of Yamamoto '865, may correspond to the electrode pad of

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Applicants' claimed invention. Similarly, the polyimide resin layer 17, as shown in FIG. 2 of Yamamoto '865, may correspond to the semiconductor protective layer of Applicants' claimed invention. The package electrode 11, as shown in FIG. 2 of Yamamoto '865 may correspond to the external electrode of Applicants' claimed invention. The first resin layer 15, as shown in FIG. 2 of Yamamoto '865, may correspond to the stress cushioning layer of Applicants' claimed invention, and the second resin layer 10, as shown in FIG. 2 of Yamamoto '865, may correspond to the surface protective layer of Applicants' claimed invention.

However, the second resin layer 10, as shown in FIG. 2 of Yamamoto '865, does not correspond to Applicants' claimed "conductor protective layer". Similarly, the polyimide layer 17, as shown in FIG. 2 of Yamamoto '865, does not serve as the stress cushioning layer as alleged by the Examiner. Rather, in Yamamoto '865, the stress cushioning layer is the first resin layer 15.

More importantly, in Yamamoto '865, none of the elements is described in anyway to address the damage due to the concentrated stress applied at the time of cutting a semiconductor wafer and at the time of mounting a semiconductor device, see page 6, lines 16-25 of Applicants' original disclosure. As a result, nowhere in Yamamoto '865 is there any disclosure or suggestion that all the elements in Applicants' claims 1, 5 and 33 are located inside of the peripheral edge of the semiconductor element. This is because typical semiconductor layers are formed across the entire wafer. This is what is shown in FIG. 13 of Yamamoto '865. Specifically, FIG. 13 of Yamamoto '865 shows that all semiconductor devices are within the square or cutting scribe lines. However, all the semiconductor layers constituting those semiconductor devices are still formed across the entire wafer (18). As shown in

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FIGs. 2-11 and FIGs. 16-22 of Yamamoto '865, all the semiconductor layers, including, for example, the polyimide resin layer and other resin layers, are formed across the wafer. Only after the resin layers are formed, will the wafer be cut into individual dices. The problem with the approach as disclosed by Yamamoto '865 is that, when the wafer is cut, a large mechanical/temperature stress is applied to the interfaces of the resin layers which, in turn, cause one or more resin layers to peel off and damage the semiconductor devices within each dice. See pages 5-6 of Applicants' original disclosure.

Likewise, nowhere in Yamamoto '865 is there any disclosure of Applicants' claimed "means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line", as expressly defined in Applicants' base claims 1, 5 and 33.

In view of the foregoing explanations and inherent deficiencies of Yamamoto '865, Applicants submit that Yamamoto '865 fails to disclose or suggest virtually all key features of Applicants' claims 1-10 and 28-36. As a result, Applicants respectfully request that the rejection of base claims 1, 5 and 33 under 35 U.S.C. §102(b) be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

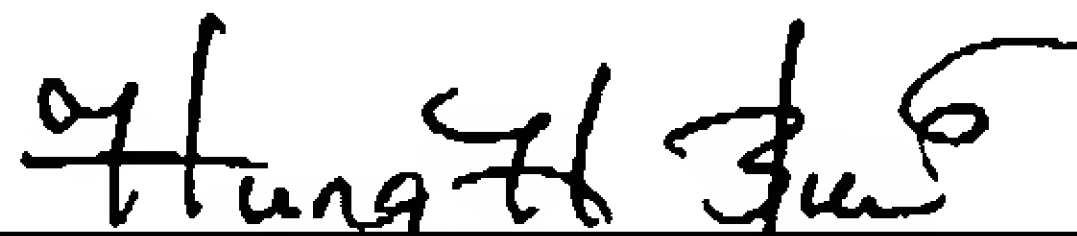
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**INTERVIEW:**

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 503.39864X00), and please credit any excess fees to said deposit account.

Respectfully submitted,  
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